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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/069,668	04/29/98	AHN	K 303.466US1

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EXAMINER	
COLEMAN, W	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/03/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/069,668	Applicant(s) AHN ET AL.	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *04 November 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I invention, claims 1-31 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 7-11, 20-22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jerome et al. U.S. Patent 5,436,496.

Jerome (496) discloses a semiconductor process substantially as claimed. See **FIGS. 2F-2M, FIG. 2F** is a cross section of die **6** with a layer **40** of polycrystalline silicon ("polysilicon") deposited over its entire surface. The polysilicon has a thickness in a range of about 4,000 Å-5,000 Å. Polysilicon layer **40** has a thin cap oxide. Oversize masks (not shown) permit formation of select P+, P-, and N+ areas in the polysilicon layer **40** by implanting both P and N type dopants through the cap oxide. The selected P+, P- and N+ areas correspond to various elements, such as an emitter, base, and collector contact, and any desired resistive elements. It is desirable to form polysilicon layer **40** with columnar grain boundaries having an average diameter of about 200 Å. Polysilicon grain boundary size is a function of temperature and doping concentration. One possible explanation of the operation of the invention is that it by

these grain boundaries that *mass transport of conductive metal atoms occurs*, although the invention is not limited to this mode of operation. A practical limit on the average grain boundary size may be the lateral dimensions of the underlying emitter. If the grain boundaries exceed the emitter dimensions, insufficient aluminum may be present above the emitter to program the fuse device. *Amorphous polysilicon or large grain polysilicon may permit sufficient mass transport of aluminum atoms to the emitter surface to enable programming.* **FIG. 2G** is a cross section of die 6 after defining and etching polysilicon layer **40**. N+ polysilicon emitter contact **42** and N+ polysilicon collector sink contact **43** respectively provide a contact to an emitter **44** (and **44'**) and to collector sink **25**. Die **6** has a silicide exclusion mask applied thereafter, followed by a final implant and anneal/oxidation step. This step drives some of the dopants from the polysilicon contact areas into the underlying epitaxial layer **15**. Creation of an emitter **44** in device **10** and an emitter **44'** in BJT **11** results from the dopants entering the epitaxial layer **15**. After annealing, an oxide etch removes the thin oxide in selected areas. **FIG. 2H** is a cross section of die **6** after oxidation by a chemical vapor deposition ("CVD") process, followed by planarization etch-back/CVD cap and contact mask/etch processes. The contact etch forms the via openings and etches through the $TiSi_2$ to the polysilicon layer **40**. To ensure the removal of all the LTO **49**, removal of some polysilicon of fuse emitter contact **42** is necessary. **FIG. 2J** is a cross section of die 6 after removal of the barrier metal from above fuse emitter contact **42**. **FIG. 2K** is a cross section of die **6** after removal of barrier metal from above fuse emitter contact **42**. **FIG. 2L** is a cross section of die **6** with exposed polysilicon emitter contacts **42**. Deposit of a firs contact metal and its subsequent masking and etching, forms metal

contacts to fuse device **10** and BJT **11**. The deposited contact metal is a mixture of aluminum, silicon, and copper. Contact metallization deposits the contact metal directly on the polysilicon emitter contact **42** over polysilicon emitter contact **44**. A layer of barrier metal between the contact metal and the polysilicon emitter contact **42** is not present. Diffusion of the aluminum metal atoms changes the nature of the polysilicon emitter contact from part contact and part emitter to a low resistance contact. The low resistance contact couples the metal contact to the shallow emitter in the epitaxial layer. Additionally, the diffusion results in the collected aluminum atoms forming a supply of contact metal atoms at the interface between the polysilicon and the epitaxial layers. During programming, some of these aluminum atoms will form an ohmic contact from the low resistance contact, through the emitter, to the base as described below. Production of an electric field results from reverse bias of the emitter-collector of the fuse device during programming. The electric field is responsible for an increase in thermal energy, which increases a solubility of silicon of the emitter region. The silicon of the emitter region forms a mixture of **Al** and **Si** which is molten at 550^0 C. Silicon combines with the supply of aluminum atoms at the interface. The thermal energy causes the mixture to melt, forming a void in the single crystal silicon through dissolution of the silicon into the aluminum. The aluminum atoms collected at the polysilicon-monocrystalline interface fill the void and provide the ohmic contact from the low resistance contact to the base. However, Jerome (496) deposits a mixture of aluminum, silicon and copper instead of aluminum only layer. In view of Jerome (496) it would have bee obvious to use only an aluminum layer to reduce material process cost in the formation of the emitter contact.

4. Claims 5 and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jerome et al. U.S. Patent 5,436,496 in view of Nakame, U.S. Patent 4,800,177.

Jerome (496) discloses a semiconductor process substantially as claimed as discussed above in claims 1-4. However, Jerome (496) fails to disclose the use of a diffusion barrier comprising at least one of the following materials: silicon carbide, a silicon oxycarbide, or a titanium nitride. Nakamae (177) discloses a semiconductor process in which a diffusion barrier comprises at least on of the following materials as claimed by Applicants. See **FIG. 4C**, platinum is then conformally deposited by, deposited onto the entire structure to form a platinum layer **30**. Heat treatment is then used at 500^0 C. for about 15 minutes to cause the platinum layer **30** to react with the polysilicon of the underlying non-doped polysilicon region **40b**, forming regions of platinum silicide which include the platinum silicide layer region 30b on the polysilicon region **40b**. Titanium-tungsten alloy is then deposited preferably using sputtering techniques on the entire surface of the resultant structure. Thereupon, aluminum is deposited on the surface of the titanium-tungsten layer. These titanium-tungsten and aluminum layers are patterned and etched to leave titanium-tungsten barrier regions including layer region **32b** on the platinum silicide layer region **38b** and wiring electrode regions including layer region **34b** of aluminum on the titanium-tungsten barrier layer region **32b** as shown in **FIG. 4D** (column 9, lines 41-64). On the other hand, the barrier layer which has been assumed to be formed by a titanium-tungsten alloy may be constructed of a metal nitride such as *titanium nitride* (TiN). In view of Nakamae (177) it would have been obvious to incorporate titanium nitride into the

Jerome (496) semiconductor process to prevent diffusion of the doped polysilicon contact to the metal emitter contact region and prevent the contact region from becoming unstable.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jerome et al. U.S. Patent 5,436,496 in view of Aboelfotoh et al. U.S. Patent 5,801,444.

Jerome (496) discloses a semiconductor device substantially as claimed as discussed in claims 1-4. However, Jerome (496) fails to disclose the use of germanium. Aboelfotoh (444) discloses the use of germanium in a semiconductor process. See FIG. 27, emitter contact at least contains n+ polysilicon and germanium. In view of Aboelfotoh (444) it would have been obvious to incorporate germanium into the Jerome (496) semiconductor process to exploit the use of technology by expanding the invention to be used in the Radio Frequency (RF) industry for high switching speeds.

6. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jerome et al. U.S. Patent 5,436,496 in view of Nakamae, U.S. Patent 4,800,177 and Aboelfotoh et al. U.S. Patent 5,801,444.

Jerome (496) in view of Nakamae (177) discloses a semiconductor process substantially as claimed as discussed above in claim 5. However, Jerome (496) in view of Nakamae (177) fail to teach the use of germanium in the semiconductor process. Aboelfotoh (444) discloses the use of germanium in a semiconductor process. In view of Aboelfotoh (444) it would have been obvious to incorporate germanium into the Jerome (496) in view of Nakamae (177) semiconductor process to exploit the use of technology by expanding the invention to be used in the Radio Frequency (RF) industry for high switching speeds.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jerome et al. U.S. Patent 5,436,496 in view of Yu et al. U.S. Patent 3,571,674.

Jerome (496) discloses a semiconductor process substantially as claimed as discussed above in claims 1-4. However, Jerome (496) fails to disclose the outdiffusion process. Yu (674) discloses a semiconductor process in which the outdiffusion process is exploited. In **FIG. 1a**, device **10** comprises a P-type monocrystalline substrate **11**, on which is grown an N-type epitaxial layer **15** of silicon. Techniques for the epitaxial growth of N-type silicon layer 15 and for the diffusion of p-type impurities into one region of this layer are well known and thus will not be described in detail (column 4, lines 5-17). It is well known in the art at the time of the invention that outdiffusion was the standard in semiconductor processing. In view of Yu (674) it would have been obvious to incorporate outdiffusion into the Jerome (496) semiconductor process to reduce equipment process cost.

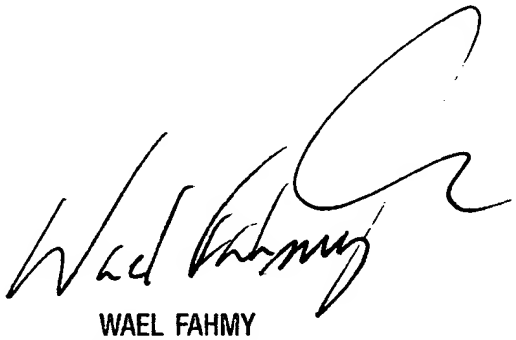
8. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on Monday-Friday from 9:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



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